at least first and second gate electrodes formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween;

a wiring for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode; and

a pixel electrode electrically connected to one of the pair of the impurity regions of the second semiconductor island;

wherein the first semiconductor island is a part of an NTFT and the second semiconductor island is a part of a PTFT.

16. (Amended) A semiconductor device comprising:

a substrate having an insulating surface;

at least first and second semiconductor islands formed directly on said insulating surface wherein each of the semiconductor islands has a channel region and a pair of impurity regions;

a first and a second gate insulating fiim formed over said semiconductor islands, respectively;

at least first and second gate electrodes formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween;

a wiring for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode;

an interlayer insulating film formed over said wiring; and

a pixel electrode formed over said interlayer insulating film and electrically connected to one of the pair of the impurity regions of the second semiconductor island,

wherein the first semiconductor island is a part of an NTFT and the second semiconductor island is a part of a PTFT.

20. (Amended) A semiconductor device comprising:

a substrate having an insulating surface;

at least first and second semiconductor islands formed directly on said insulating surface wherein each of the semiconductor islands has a channel region and a pair of impurity regions;

a first and a second gate insulating film formed over said semiconductor islands, respectively;

at least first and second gate electrodes formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween;

a wiring for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode;

a surface smoothing film formed over said wiring; and

a pixel electrode formed over said surface smoothing film and electrically connected to one of the pair of the impurity regions of the second semiconductor island,

wherein the first semiconductor island is a part of an NTFT and the second semiconductor island is a part of a PTFT.